IN THE CLAIMS

1. (Original) A content addressable memory (CAM) apparatus comprising:

an array of CAM cells;

a select circuit adapted to generate a plurality of select signals each indicative of a segment of input data provided to the CAM apparatus; and

switch circuitry including a plurality of programmable switch circuits each programmable to output a respective bit of the input data as a comparand bit for the array of CAM cells in response to one of the select signals.

2. (Original) The CAM apparatus of claim 1, wherein the select circuit comprises:

a memory storage circuit for storing programmed segment information; and

a compare circuit coupled to the memory storage circuit to compare the programmed segment information with input segment information to generate one of the select signals.

3. (Original) The CAM apparatus of claim 2, wherein the compare circuit and the memory storage element form a CAM cell.

4. (Original) The CAM apparatus of claim 1, wherein the switch circuitry comprises a cross-bar switch.

5. (Original) The CAM apparatus of claim 1, wherein the switch circuitry comprises L rows of L programmable switch circuits coupled to receive L input bits of the input data and L select signals from the select circuit.

6. (Original) The CAM apparatus of claim 5, wherein the L inputs bits are one of N segments of M input bits where M is equal to N multiplied by L.

7. (Original) The CAM apparatus of claim 1, further comprising a comparand storage element coupled between the plurality of programmable switch circuits and the array of CAM cells, the comparand storage element to store the comparand input bit.

8. (Original) The CAM apparatus of claim 7, further comprising a global mask register coupled between the comparand storage element and the array of CAM cells.

9. (Original) The CAM apparatus of claim 1, further comprising a program circuit coupled to the switch circuits to program the plurality of programmable switch circuits.

10. (Original) The CAM apparatus of claim 1, wherein the input bit has a first bit position in an input data and the comparand bit has a second, different bit position in comparand data for the array of CAM cells.

11. (Original) A content addressable memory (CAM) apparatus comprising:

an array of CAM cells;

means for generating a plurality of select signals each indicative of a segment of input data provided to the CAM apparatus; and

switch circuitry including a plurality of programmable switch circuits each programmable to output a respective bit of the input data as a comparand bit for the array of CAM cells in response to one of the select signals.

12. (Original) The CAM apparatus of claim 11, wherein the switch circuitry comprises a cross-bar switch.

13. (Original) A content addressable memory (CAM) apparatus comprising:

X CAM array blocks each having R rows of L CAM cells, where X, R, and L are integers greater than one and wherein the CAM apparatus has a total of R multiplied by X rows of CAM cells;

X select circuits each adapted to generate a plurality of select signals each indicative of a segment of input data provided to the CAM apparatus; and

X switch circuits each including a plurality of programmable switch circuits each programmable to output a respective bit of the input data as a comparand bit for a corresponding one of the CAM array blocks in response to one of the select signals.

14. (Original) The CAM device of claim 13, wherein at least one of the select circuits comprises:

a memory storage circuit for storing programmed segment information; and

a compare circuit coupled to the memory storage circuit to compare the programmed segment information with input segment information to generate one of the select signals.

15. (Original) The CAM apparatus of claim 14, wherein the compare circuit and the memory storage element form a CAM cell.

16. (Original) The CAM apparatus of claim 13, wherein at least one of the switch circuits comprises a cross-bar switch.

17. (Original) The CAM apparatus of claim 13, wherein at least one of the switch circuits comprises L rows of L programmable switch circuits coupled to receive L input bits of the input data and L select signals from the corresponding select circuit.

18. (Original) The CAM apparatus of claim 17, wherein the L inputs bits are one of N segments of M input bits where M is equal to N multiplied by L.

19. (Original) The CAM apparatus of claim 13, further comprising at least one program circuit coupled to at least one of the switch circuits to program the plurality of programmable switch circuits.

20. (Original) The CAM apparatus of claim 13, wherein the input bit has a first bit position in an input data and the comparand bit has a second, different bit position in comparand data.

21. (Original) A content addressable memory (CAM) apparatus comprising:

an array of CAM cells having Z rows of X segments of L CAM cells, where X, Z, and L are integers greater than one and wherein the CAM apparatus has a total of Z rows of CAM cells;

X select circuits each adapted to generate a plurality of select signals each indicative of a segment of input data provided to the CAM apparatus; and

X switch circuits each including a plurality of programmable switch circuits each programmable to output a respective bit of the input data as a comparand bit for a corresponding one of the CAM array blocks in response to one of the select signals.

22. (Original) The CAM device of claim 21, wherein at least one of the select circuits comprises:

a memory storage circuit for storing programmed segment information; and

a compare circuit coupled to the memory storage circuit to compare the programmed segment information with input segment information to generate one of the select signals.

23. (Original) The CAM apparatus of claim 22, wherein the compare circuit and the memory storage element form a CAM cell.

24. (Original) The CAM apparatus of claim 21, wherein at least one of the switch circuits comprises a cross-bar switch.

25. (Original) The CAM apparatus of claim 21, wherein at least one of the switch circuits comprises L rows of L programmable switch circuits coupled to receive L input bits of the input data and L select signals from the corresponding select circuit.

26. (Original) The CAM apparatus of claim 25, wherein the L inputs bits are one of N segments of M input bits where M is equal to N multiplied by L.

27. (Original) The CAM apparatus of claim 21, further comprising at least one program circuit coupled to at least one of the switch circuits to program the plurality of programmable switch circuits.

28. (Original) The CAM apparatus of claim 21, wherein the input bit has a first bit position in an input data and the comparand bit has a second, different bit position in comparand data.

29. (Original) A method comprising:

programming a select circuit to generate a plurality of select signals each indicative of a segment of input data provided to a content addressable memory (CAM) apparatus having an array of CAM cells; and

programming switch circuitry to output a respective bit of the input data as a comparand bit for the array of CAM cells in response to one of the select signals.

30. (Original) A method comprising:

receiving a plurality of segments of input data in a content addressable memory (CAM) apparatus having an array of CAM cells;

receiving segment information indicative of which segment of the input data is received at any given time; and

selectively enabling, in response to the segment information, programmed switch circuitry to filter at least one bit of the input data to generate at least one comparand bit for the array of CAM cells.

31. (Original) The method of claim 30, wherein the selectively enabling further comprises selectively enabling at least one programmed switch circuit to couple one bit of the input data to at least one bit position of a comparand storage element.

32. (Original) The method of claim 30, further comprising comparing the comparand bit with data stored in the array of CAM cells.

33. (Currently Amended) A method, comprising:

receiving first data on an input bus of a content addressable memory (CAM)~~CAM~~ device for performing a write operation; and

receiving second data on the input bus of the CAM device for performing a compare operation.

34. (Previously Presented) The method of claim 33, further comprising time multiplexing the receipt of the first data and the second data.

35. (Previously Presented) The method of claim 33, further comprising transmitting the first data received on the input bus to read/write circuitry in the CAM device.

36. (Previously Presented) The method of claim 33, further comprising transmitting the second data received on the input bus to a filter circuit in the CAM device.